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TM-1326
1731.010

A PROGRAMMABLE HIGH POWER BEAM DAMPER FOR THE TEVATRON*

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June 1985

*Submitted to the 1985 Particle Accelerator Conference (NPS), Vancouver, British Columbia, Canada, May 13-16, 1985.

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Abstract

A bunch-by-bunch beam damper has been developed for the Fermilab Tevatron. The system reduces betatron oscillation amplitudes and incorporates some useful machine diagnostics. The device is programmable via look-up tables so the output is an arbitrary function, on a bunch-by-bunch basis, of the beam displacement. We are presently using this feature to measure the betatron tune throughout the acceleration cycle.

Introduction

At high beam intensity the interaction of the beam with beam induced eddy currents in the beam pipe can cause instabilities which limit the maximum intensity of the Tevatron. These instabilities can be damped with an active damper which measures the beam displacement and then generates a voltage pulse which deflects the beam back towards the beam axis. The beam damper consists of a beam position detector, digital processor, diagnostic electronics, 5 kW power amplifiers, and an electromagnetic deflector (Fig. 1). The 53 MHz digital processor maps the displacement signal for each bunch into one of 16 deflection voltage functions. All digital signal processing is done in real time at a 53 MHz rate. The front-end electronics performs an integration of the 2 ns detector pulses so its frequency response is especially broad.

The maximum deflection voltage available is 3 kV, which limits the damping rate to 1.4% per beam turn. The position detector and beam deflector are separated an odd number of betatron wavelengths; $\lambda/4$ in the vertical damper and $3\lambda/4$ in the horizontal damper.

Functional Description

The detector is a Tevatron Beam Position Monitor stripline (ref. 1) increased to 1 m length. Each stripline plate produces a 2 ns bipolar doublet pulse. The pulse amplitudes of the two plate signals, A and B, are related to the transverse bunch position and the number of particles in the bunch. To enhance fidelity, the signals are subtracted and summed at the detector and then transmitted to the service building. These combined signals retain the bipolar doublet character of the raw ones. The duration of the doublet pulses is so short that direct A/D sampling would be very difficult. Instead, a fast integration and dump technique is used to provide a flat topped pulse.

Integration takes place by charging a 20 pF holding capacitor from a voltage-controlled current source. The capacitor is largely discharged by the complementary half of the doublet. To remove any remaining charge, a SPST (600 ps time constant) diode switch is operated synchronously between pulses.

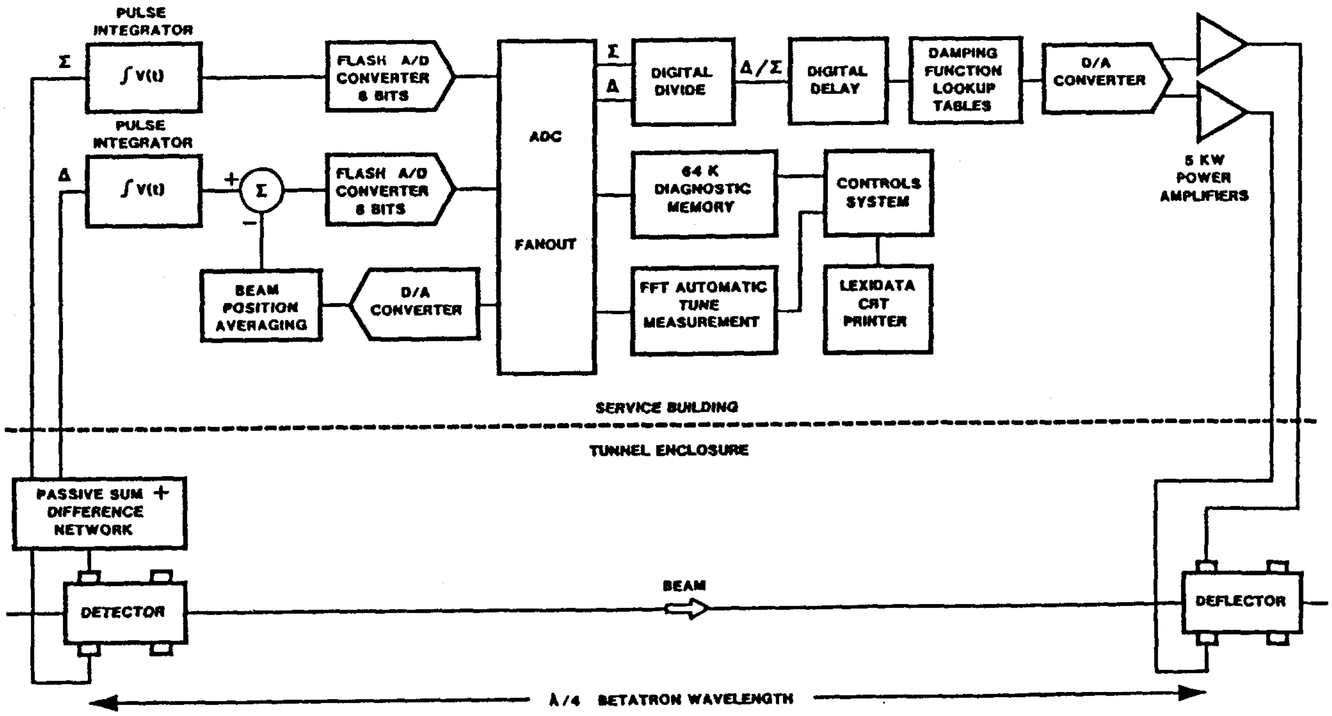

Figure 1 Block Diagram of Beam Damper

*Operated by Universities Research Inc., under contract with the U.S. Department of Energy

The resulting integrated pulse is 6.6 ns long, twice the flight time of the detector.

Available A/D converters inherently have high input capacitance because the analog input is fanned out into many comparators. This problem was exacerbated by stacking four 6-bit components to yield a composite 8-bit converter. To drive the highly capacitive (140 pF) load, a 6 ohm output impedance buffer was designed.

Digital Processing System

The digital processing system is a table driven processor implemented in MECL 10K and 10KH logic. The function of this section is 1)to divide the A-B signal by the total bunch intensity, 2)to delay the signal until the beam comes around the ring again, and 3)to determine a deflector plate voltage which will damp the betatron oscillation.

We augmented these basic operations by providing a choice of 16 different plate voltage functions that can be applied to the beam. Each function is stored in a 256 X 8 bit look-up table so a wide variety of voltage functions are possible. Each bunch in the ring can be assigned to any one of the 16 voltage functions. Thus, one can remove 5 bunches from the machine by selecting an anti-damping function for the 5 bunches and damping for the rest. Another function is to antidamp at low betatron amplitudes and damp at large betatron amplitudes. This has the effect of exciting a constant amplitude betatron oscillation in the selected bunches. By Fourier analyzing the A-B signal one can measure the machine tune. This can be done using only one bunch. A more detailed description of the digital processor can be found in Ref. 2.

The division module described in Ref. 2 used logarithm and antilogarithm tables. This has now been replaced by a 16K X 8 bit memory. The 7 bit A+B signal and the 7 bit magnitude of the A-B signal are combined to form a 14 bit memory address. The memory contains the quotient. If A-B is negative, the results are complemented. The use of a memory table allows one to treat special cases such as A-B > A+B in a very easy way. One can also partially compensate for decreased signal to noise at small signal levels by scaling the quotient down when A+B is less than a specified value.

Another feature that has been expanded is the ability to select various damping functions at different times in the cycle. This is achieved by putting gates on the four bit bunch function code. This four bit code forms the upper four bits of a 4K X 8 bit memory which contains the various voltage functions. By gating the most significant bit off one converts functions 8-15 into 0-7. The original design had only the most significant bit gatable. This has been expanded to allow the three most significant bits to be gatable.

Diagnostic Memory

Position data from the damper system can be stored in a 64K fast memory system. This CAMAC-based memory consists of four 16K memory boards that are driven by a two board controller. The controller receives the first bunch pulse, 53 MHz clock and the position data as input. Output data are interleaved in the four memory boards so that MOS memory chips could be used (55 ns cycle time). The 53MHz clock increments a bunch-number counter that addresses a 2K X 1 bit memory to determine if data from a particular bunch is to be stored. This memory allows any arbitrary pattern of bunch data to be stored in the 64K memory. Both the data and the associated bunch number are stored.

Additional features of the memory system allow operation in either a linear or circular buffer mode, prescaling of the bunch number, and starting and stopping data storage by timing pulses, beam abort triggers or program control. The circular buffer mode is useful for examining beam motion prior to a beam induced abort.

An auxiliary 68000/VMEbus-based microprocessor system can be used with the damper to measure the horizontal and vertical fractional tune of the Tevatron. If position data for a single bunch is collected for many successive turns, a fast fourier transform of those data can give a spectrum that shows a peak at the frequency corresponding to the tune of the accelerator. The damper may be operated to maintain a coherent betatron oscillation in one of the 1113 bunches. Data from that bunch is selected by a CAMAC card and output to a 1K FIFO memory located in the VMEbus crate. A DMA controller transfers the block of 1024 position readings to an array processor memory. An FFT is performed on these data and the resulting 512 amplitudes represent fractional tune values in the range 0.0 to 0.5. The array processor searches for the peak value and both the peak and the full spectrum are stored in a 2 megabyte RAM card. Data from both the horizontal and vertical damper systems are processed as described 15 times per second, resulting in a nondestructive 15 Hz tune measurement for both planes. In operation, the 2 MB memory contains a record of the tunes as a function of time and the FFT results for an entire Tevatron cycle. Data from the last cycle are overwritten with data from the current cycle as new data are processed. The fractional tune values are output as D/A voltages for the Tevatron control system. The tune results are then available to be plotted as normal data on the control system consoles. Live input position data, FFT results, stored tune and FFT spectra can be plotted on a color graphics display by a second 68000 system located in the Main Control Room. Communication between the MCR and the RF Service Building (approx. 1.6 Km) is by way of an ARCnet local area network.

Power Amplifier and Deflector

Each plate of the Deflector is driven by a distributed amplifier using 24 Eimac 4CW800F tetrode tubes. Each of these amplifiers is organized as two separate 12.5 ohm grid lines and a common 50 ohm anode line. The measured characteristics are 200 MHz bandwidth and 3.7 ns 10-90% rise time with 10% overshoot. The overshoot and ringing can be reduced at the expense of rise time by introducing a delay in one of the grid lines. The maximum plate to plate voltage in the deflector is equal to the anode supply voltage of 1.5 kV. This provides a deflection equivalent of 3 kV, taking into consideration the sum of E and H fields in the deflector. All four amplifiers, two horizontal and two vertical, share a common anode power supply.

The deflector is configured as a balanced stripline with 50 ohms impedance plate to ground when driven differentially. The plates are 140 cm long, 10.8 cm wide and have a 6.35 cm separation. The deflection pulse energy travels along the plates in the direction opposing the beam. With this geometry the kick imparted to the beam due to the magnetic field is essentially equal in magnitude and direction to the kick provided by the electric field. The plate length is selected to be less than 1/2 (bunch spacing-bunch length-amplifier rise time). Figure 2 shows the affect of anti damping 3 bunches as a function of the number of turns from the start of the anti damping operation.

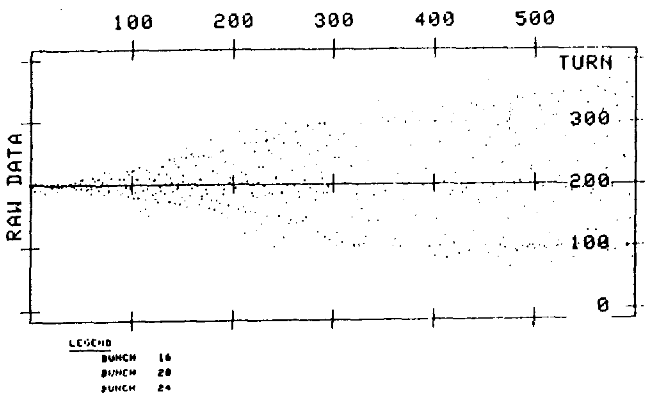

Figure 2

Bunch Positions for Three Antidamped Bunches
vs. Machine Turn

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